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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,433	05/09/2001	Jun Koyama	0756-2307	2113

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EXAMINER	
KOVALICK, VINCENT E	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,433	KOYAMA ET AL.	
	Examiner	Art Unit	
	Vincent E Kovalick	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-44 and 55-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-44,59 and 60* is/are allowed.

6)☒ Claim(s) *55-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's Amendment and RCE dated December13, 2004 and Applicant's Supplement Amendment, dated December 29, 2004, in response to USPTO Final Office Action dated August 10, 2004.

The cancellation of claims 1-32 and 45-54; the amendments to claims 35, 55 and 57; and Applicant's remarks have been noted, given full consideration and entered in the record.

Applicant remarks regarding claims 55 and 57 indicating "Sato does not teach or suggest providing a dateline side drive circuit, a memory and a memory control circuit over a same substrate or casting a pixel matrix and associated memory and control logic on a same substrate" are rendered moot with the introduction of new prior art used in the rejection of claims said claims 55 and 57.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 55-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama (USP 5,793,344), taken with Furukawa (USP 6,040,826).

Relative to claims 55 and 57, Koyama **teaches** a substrate based system for correcting display device and method for correcting the same (col. 2, lines 57-67 and col. 3, lines 1-27); Koyama further **teaches** a device comprising a pixel portion over a substrate; a data line side driver circuit provide over the substrate and operationally connected to the pixel portion; a memory portion provided over the substrate and operationally connected to the data line side driver circuit; a memory control circuit provided over the substrate and operationally connected to the memory portion (col. 3, lines 54-64; col. 6, lines 42-50 and Figs. 1 and 6).

Koyama **does not specifically teach** the signal flow wherein an image signal is transferred to said memory control circuit, from said memory control circuit to said memory portion, and from said memory portion to said data line side drive circuit. Koyama teaches a system for correcting a display device.

Furukawa **teaches** a driving circuit for driving a simple matrix type display apparatus (col. 3, lines 48-67 and col. 4, lines 1-58); Furukawa further **teaches** the system signal flow wherein an image signal is transferred to said memory control circuit, from said memory control circuit to said memory portion, and from said memory portion to said data line side drive circuit (col. 6, lines 30-55 and Fig. 3). Referring to Fig. 3, the image signal comes into the line buffer (item 2) portion of the memory control circuit (item 4), from the memory control circuit to said memory portion (item 3), and from said memory portion to said data line side driver circuit (item 6). Further, the memory control circuit operationally connected to the data line side circuit is accomplished through the frame buffer (item 3) and Orthogonal transformation circuit (item 51) to the data side driver circuits (item 6).

It would have been obvious to a persons of ordinary skill in the art at the time of the invention to provide to the device as taught by Koyama the feature as taught by Furukawa in order to interconnect the elements mounted on the said substrate in the manner necessary to control the data flow from the image signal from the input, through the memory control circuit into the memory unit and onto the data line said driver circuit.

Regarding claims 56 and 58 Koyama further **teaches** the device memory being a (EEPROM) selected from the group consisting of SRAM, DRAM AND EEPROM (col. 6, lines 19-28).

Allowable Subject Matter

4. Claims 33-44 and 59-60 are allowed.

5. The following is an examiner's statement of reasons for allowance:

Regarding claim 33, the major differences between the teachings of the prior art of record (USP 5,793,344, Koyama and USP 6,040,826,Furukawa) and that of the instant invention is that said prior art of record **does not teach** a semiconductor device comprising at least a pixel portion, a data line side driver circuit, a scanning line side driver circuit and a memory portion wherein the pixel portion is formed over a first substrate, the data line side driver circuit and said memory portion are formed over a second substrate and said scanning line side drive circuit is integrally formed over a third substrate.

Relative to claim 59, major differences between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a

device comprising an input terminal; a first control circuit operationally connected to the input terminal; a second control circuit operationally connected to the first control circuit; at least one first memory operationally connected to the first control circuit; a memory control circuit operationally connected to the second control circuit; a memory portion operationally connected to the memory control circuit; a data line side driver circuit operationally connected to the memory portion; and a pixel portion operationally connected to the data line side driver circuit, wherein all of the first control circuit, the second control circuit, the first memory, the memory control circuit, the memory portion, the data line side driver circuit and the pixel portion are provided adjacent to a same substrate.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,798,394	Chimura
U. S. Patent No.	6,069,793	Maruyama et al.
U. S. Patent No.	5,841,497	Sato et al.

Responses

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent E. Kovalick
January 31, 2005

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